10xEngineers' RISC-V IOPMP IP

Accelerate Your Time-to-Market with High-Quality IP

IP Highlights

- **Fully configurable** – 28 configurable design parameters enabling optimal trade-offs across area, power, latency and throughput
- **Complete feature set** – implements all mandatory and optional features
- **High-performance design** fully pipelined design optimized for high-frequency, single-cycle throughput
- **Inline integration model** – processes transaction requests and responses directly through the IOPMP
- **Flexible addressing** – Four address modes, with minimum granularity of 8 bytes
- **Robust protection** – triggers interrupts and detailed violation logging
- **Outstanding request handling** – up to 32 concurrent requests
- **Scalable resources** – up to 63 MDs
- **Customizable RRIDs** – up to 64 RRIDs, with flexible mapping to any MD
- **Customizable Array entries** – up to 128 entries with up to 48 priority entries
- **Tapeout ready** – verified with a UVM test bench, RAL, and C-reference model, 100% coverage closure
- **Technology optimized** – synthesized for 12nm/1GHz

About 10xEngineers

We specialize in RISC-V design and verification, delivering IP blocks and security solutions that power the next generation of SoCs. Our RISC-V IOPMP is part of a growing portfolio of trusted IPs enabling safe, secure, and scalable designs.

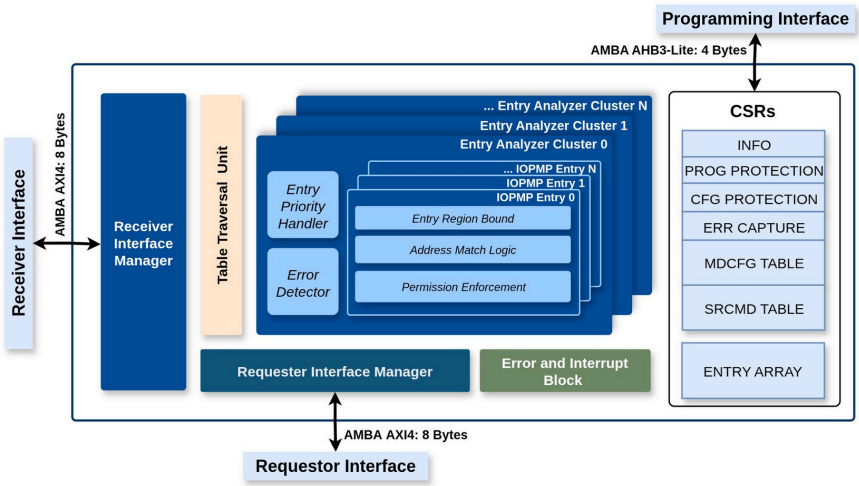
CONTACT US

What is an IOPMP?

The **I/O Physical Memory Protection (IOPMP)** unit is a hardware-based access control mechanism designed to safeguard memory regions in RISC-V SoCs. It ensures **only authorized devices and masters** can access sensitive memory areas, enabling secure and reliable system operation.

Key Features

- **Fine-Grained Memory Protection** - Define multiple memory regions with configurable read, write, and execute permissions.
- **Hardware-Enforced Security** - Blocks unauthorized DMA and peripheral access before they can compromise system integrity.
- **Flexible Configuration** - Supports dynamic reconfiguration for multi-tenant or virtualization scenarios.
- **Low Latency & Lightweight** - Designed to minimize performance overhead while maximizing system resilience.
- **RISC-V Standards Aligned** - Fully compatible with the latest RISC-V specifications and open hardware ecosystem.



10xEngineers' RISC-V IOPMP Block Diagram

Customization & Services

10xEngineers delivers a complete, pre-verified IP package ready for seamless SoC integration. Our expert team provides customization services to match your specific design requirements helping you:

- Reduce integration effort
- Minimize design risk
- Accelerate time-to-market

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